PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-324686
(43)Date of publication of application : 24.11.2000

(51)Int.Cl. H02J 1/00
H02M 3/28

(21)Application number : 11-133976
(22)Date of filing : 14.05.1999

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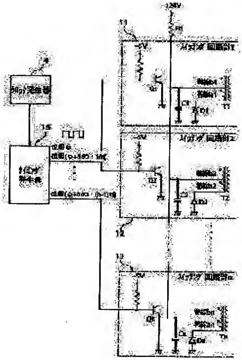
(54) TRANSFORMER DRIVE CIRCUIT

(57)Abstract:

PROBLEM TO BE SOLVED: To prevent the total of ripple current values flowing through an electrolytic capacitor for composing each switching circuit part from increasing as compared with a case where there is only one switching circuit part and use only the minimum, required capacity of the electrolytic capacitor even when a plurality of switching circuit parts are installed.

SOLUTION: Based on a clock signal generated by a clock generator 14, a timing generator 15 generates a plurality of clock signals with each different phase and supplies them to switching transistors Q1-Qn. The switching transistors Q1-Qn turn on or turn off based on each clock signal and excite transformers T1-Tn. An averaged ripple current is supplied to electrolytic capacitors C1-Cn.



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CLAIMS

[Claim(s)]
[Claim 1] In the transformer drive circuit of a separate excitation system which carries out the excitation drive of two or more transformers Corresponding to two or more transformers connected to the same power source, and said two or more transformers, it is prepared, respectively. Two or more capacitors which perform rectification and **** of the electrical potential difference by which the TORANSUHE input of the correspondence is carried out, and perform the storage of energy from supply and this transformer of the energy of this TORANSUHE, The switching transistor which is prepared corresponding to said two or more transformers, respectively, and drives the transformer of correspondence, Based on the clock signal generated by clock generation means to generate at least one clock signal, and said clock generation means The transformer drive circuit characterized by having the timing control means which generates two or more clock signals of a mutually different phase, and is supplied to the switching transistor of correspondence, respectively.
[Claim 2] By said clock generation means generating one clock signal, said timing control means does n division into equal parts of the period T of a transformer drive according to the quantity n of two or more of said transformers, time amount T/n is obtained, and it is the transformer drive circuit according to claim 1 characterized by making it delayed, creating n clock signals, and supplying the switching transistor of correspondence, respectively time amount T/n every about said clock signal.
[Claim 3] Said clock generation means is a transformer drive circuit according to claim 1 characterized by generating two or more clock signals with which phases differ.
[Claim 4] The transformer drive circuit according to claim 1 to 3 characterized by supplying each high voltage which said two or more transformers generate to image formation equipment.

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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the transformer drive circuit of the separate excitation system used for image formation equipments, such as a laser beam printer which adopts an electrophotography process method, a reproducing unit, and facsimile apparatus, about the transformer drive circuit of a separate excitation system.
[0002]
[Description of the Prior Art] Generally, the image formation equipment which adopted the electrophotography method is equipped with the high-voltage transformer assembly, and offers fundamentally the primary electrification bias for which this high-voltage transformer assembly is needed in image formation equipment, development bias, imprint bias, fixing bias, etc.
[0003] By the way, needed high-voltage bias is complicated with colorization of image formation equipment etc., and two or more various bias is needed. For example, imprint material, such as paper, is made to stick to an imprint drum or an imprint belt, and adsorption bias, separation electric discharge bias, etc. are needed in the color laser printer of a configuration of performing separation fixing after the imprint of a toner.
[0004] Moreover, in the color laser printer in which a middle imprint object is included, the sequential imprint of the toner image developed on the image bearing body is carried out for every color of yellow, a Magenta, cyanogen, and black, and it imprints secondarily to imprint material collectively after that. For this reason, the secondary imprint bias imprinted again is needed for imprint material from the primary imprint bias which imprints imprint bias on a middle imprint object from an image bearing body, and a middle imprint object.
[0005] Furthermore, four latent-image formation processes and four development processes may be constituted independently for every color, respectively, and primary electrification bias and four development bias are also independently needed in a high-speed color laser printer, in this case in many cases, respectively. Thus, it followed on colorization of image formation equipment etc., and the high-voltage bias configuration is complicated and diversified.
[0006] Here, the configuration of the conventional transformer drive circuit used for a high-voltage transformer assembly is explained.
[0007] Drawing 5 is the block diagram showing the transformer drive circuit in conventional image formation equipment.
[0008] Among drawing, two or more switching circuit sections (1-n) 51-53 are formed mutually-independent, and a separate excitation drive is carried out with the same clock generation vessel 54, respectively. n is two or more integers. The clock generation machine 54 generates the clock signal of predetermined frequency and duty, the generated clock signal is supplied common to all the switching circuit sections from switching circuit section (1) 51 to the switching circuit section (n) 53, and each switching circuit section carries out the excitation drive of each transformers T1-Tn.
[0009] The input coil side serves as a bifilar wound, and each transformers T1-Tn form the snubber

circuit, respectively with Diodes D1-Dn and Coils a1-an. It connects with power-source +24V and electrolytic capacitors C1-Cn, respectively, and each common terminal of an input coil shows the current wave form where it flows to rectification and smooth **** crack **************** C1-Cn of the current supplied to Transformers T1-Tn to drawing 6 . Moreover, a ripple current path is shown in drawing 7 . In addition, drawing 7 shows the example of n= 2.

[0010] In the switching circuit section 51 shown in drawing 7 , a current ib1 flows to the coil b1 of a transformer T1 at the time of ON of a switching transistor Q1. At the time of OFF of a switching transistor Q1, a current ia1 flows to the coil a1 of a transformer T1. A current ia1 is the charging current which returns the energy absorbed in the snubber circuit to a power source. Moreover, when an above-mentioned snubber circuit operates, the collector voltage of a switching transistor Q1 is clamped on the electrical potential difference which becomes by about 2 twice power-source +24V.

[0011] In an electrolytic capacitor C1, it flows as an object for supply of the power with which a current ic1 is consumed by transformer T1 output side in addition to the above-mentioned current ia1 and current ib1. However, a current ic1 is very small as compared with the above-mentioned current ia1 or a current ib1, and the great portion of ripple current is occupied with the current ia1 and the current ib1.

[0012] The above is the same also in the switching circuit section of further others also in the switching circuit section 52, although the switching circuit section 51 was made into the example and explained.

[0013] Each ripple current wave which flows to each electrolytic capacitors C1-Cn is shown in drawing 6 (A), and the sum total wave of each ripple current in n= 2 is shown in drawing 6 (B). Since the ripple current of in phase and this period is flowing in each electrolytic capacitors C1-Cn, the sum total ripple current value [drawing 6 (b)] in n= 2 increases the twice [about] of the independent ripple current value [drawing 6 (A)] in n= 1.

[0014]

[Problem(s) to be Solved by the Invention] However, in the conventional transformer drive circuit shown in drawing 5 , since two or more transformers were driven based on the same clock signal, the ripple current value which Currents ia1-ian and Currents ib1-ibn flow with the same period and the same phase to each electrolytic capacitors C1-Cn, respectively, are totaled by each electrolytic capacitors C1-Cn, respectively, and flows was increased.

[0015] That is, in the conventional transformer drive circuit, fundamentally, since a ripple current value served as several times as many installation of the switching circuit sections 51-53 as this, the switching circuit sections 51-53 had to be alike, respectively, and it had to have the electrolytic capacitor of comparatively big capacity value.

[0016] provide this invention with a necessary minimum electrolytic capacitor capacity while making it the sum total of a ripple current value which flows to the electrolytic capacitor which constitutes each switching circuit section not increase as compared with the case where the number of the switching circuit sections is one, when it is made in view of such a trouble and two or more switching circuit sections are installed -- ** -- it aims at offering the transformer drive circuit made like.

[0017]

[Means for Solving the Problem] In the transformer drive circuit of a separate excitation system which carries out the excitation drive of two or more transformers according to invention according to claim 1 in order to attain the above-mentioned purpose Corresponding to two or more transformers connected to the same power source, and said two or more transformers, it is prepared, respectively. Two or more capacitors which perform rectification and **** of the electrical potential difference by which the TORANSUHE input of the correspondence is carried out, and perform the storage of energy from supply and this transformer of the energy of this TORANSUHE, The switching transistor which is prepared corresponding to said two or more transformers, respectively, and drives the transformer of correspondence, Based on the clock signal generated by clock generation means to generate at least one clock signal, and said clock generation means Two or more clock signals of a mutually different phase are generated, and it is characterized by having the timing control means supplied to the switching transistor of correspondence, respectively.

[0018] Moreover, according to invention according to claim 2, it is characterized by for said clock

generation means generating one clock signal, and said timing control means doing n division into equal parts of the period T of a transformer drive according to the quantity n of two or more of said transformers, obtaining time amount T/n, delaying said clock signal time amount T/n every, creating n clock signals, and supplying the switching transistor of correspondence, respectively.
[0019] According to invention according to claim 3, said clock generation means is characterized by generating two or more clock signals with which phases differ.
[0020] Furthermore, according to invention according to claim 4, it is characterized by supplying each high voltage which said two or more transformers generate to image formation equipment.
[0021]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.
[0022] (Gestalt of the 1st operation) Drawing 1 is the circuit diagram showing the outline configuration of the transformer drive circuit concerning the 1st operation gestalt of this invention. This transformer drive circuit supplies the high voltage to image formation equipment.
[0023] In this drawing, a transformer drive circuit consists of the n switching circuit sections (1-n) 11-13 (n is two or more integers) by which a separate excitation drive is carried out and which were prepared mutually-independent, clock generation machines 14, and timing generators 15.
[0024] The switching circuit section (1) 11 consists of a transformer T1, diode D1, an electrolytic capacitor C1, and switching transistor Q1 grade. A switching transistor Q1 is turned on and off according to the clock signal inputted into the base, and performs flow cutoff of the current supplied to a transformer T1 from a power source. The input coil side serves as a bifilar wound, and the transformer T1 forms the snubber circuit with diode D1 and a coil a1. The common terminal of an input coil is connected to power-source +24V and an electrolytic capacitor C1, respectively, and an electrolytic capacitor C1 performs rectification and **** of the current supplied to a transformer T1, and accumulates supply of the energy to a transformer T1, and energy from a transformer T1.
[0025] The switching circuit sections (2-n) 12-13 are also the respectively same configurations as switching circuit section (1) 11, and perform the same actuation.
[0026] The clock generation machine 14 generates a predetermined frequency and the clock signal of duty. A timing generator 15 makes a period time amount acquired by carrying out n division of the transformer drive period T according to the quantity n of the switching circuit sections 11-13, generates a delay signal, and outputs in order the clock signal which begins from the same phase location for every timing of this delay signal to the switching circuit sections 11-13. In other words, a timing generator 15 delays the clock signal generated with the clock generation vessel 14 a T/n period every, generates n clock signals, and outputs them to the circuit where the switching circuit sections 11-13 correspond, respectively. At this time, the phase of the clock supplied to the switching circuit section (m) is expressed with {phi+360degreex(m-1)/n}. In addition, m is the integer of the arbitration which fills 1 <=m<=n. Hereafter, it explains, using m similarly.
[0027] Drawing 2 is drawing showing the ripple current wave which flows to the electrolytic capacitor Cm when a switching circuit (m) drives independently with the clock signal of a phase {phi+360degreex (m-1)/n}. However, it shall not connect for convenience other than Capacitor Cm.
[0028] The period of the ripple current is T. The time delay in the timing generator 15 of a clock signal inputted into the switching circuit section (m) can be expressed as x(m-1) T/n on the basis of the clock signal inputted into switching circuit section (1) 11.
[0029] Drawing 3 is drawing showing the sum total wave of the ripple current which flows to each electrolytic capacitor Cm in n= 2, and 3 and 4. Drawing 2 and drawing 3 are shown by the same scale.
[0030] In the conventional transformer drive circuit, the sum total ripple current [drawing 6 (B)] in n= 2 was twice [about] the ripple current [drawing 6 (A)] in n= 1. However, a ripple current value [in / at the gestalt of this operation / n= 2] [drawing 3 (A)] is almost changeless as compared with the ripple current value at the time of n= 1 (drawing 2), although the period of the ripple current to which it flows changes to T/2. In the ripple current value [drawing 3 (B)] in n= 3, the period of the ripple current to which it flows becomes T/3, and the ripple current decreases conversely. In the ripple current value

[drawing 3 (C)] in n= 4, the period of the ripple current to which it flows becomes T/4, and the ripple current decreases further.
[0031] That is, according to the gestalt of this operation, a period serves as T/n and a current value can make the sum total of a ripple current value which flows to an electrolytic capacitor Cm when the switching circuit section is constituted from n pieces below the ripple current value in n= 1. And this ripple current value decreases, so that it enlarges n.
[0032] Here, why the sum totals of the ripple current decrease in number is explained.
[0033] About the case of n= 2, each transformer Tm and the current which flows to each electrolytic capacitor Cm (m is the integer of 1 <=m<=n and arbitration) are shown in drawing 4 . Since the phase of the clock signal supplied to each switching circuit section (m) is expressed with {phi+360degreex(m-1)/n}, each clock signal supplied to switching circuit section (1) 11 and switching circuit section (2) 12 became a phase phi and a phase (phi+180 degrees), and 180 degrees of phases have shifted.
[0034] Therefore, the current ib1 which each switching transistor Qm which constitutes each switching circuit section (m) repeats ON-OFF to timing which is mutually different, and flows at the time of ON of a switching transistor Q1 comes to be supplied in the part by the current ia2 on which a switching transistor Q2 flows at the time of OFF. Moreover, it comes to supply the current ia1 which flows at the time of OFF of a switching transistor Q1 to the current ib2 on which a switching transistor Q2 flows the part at the time of ON.
[0035] That is, it made it possible to equalize the ripple current with the whole electrolytic capacitor by preparing time difference (phase) in each ripple current which was flowing in phase and this period to each electrolytic capacitor Cm conventionally.
[0036] (Gestalt of the 2nd operation) Drawing 8 is the circuit diagram showing the outline configuration of the transformer drive circuit concerning the gestalt of the 2nd operation.
[0037] A transformer drive circuit is constituted from the switching circuit sections (1-n) 51-53 (n is two or more integers), the clock generation machine 54, and a timing generator 55 by the gestalt of the 2nd operation as well as the gestalt of the 1st operation.
[0038] The clock generation machine 54 generates a k piece clock signal with a mutually different frequency and duty in each (k is the natural number of arbitration). A timing generator 55 generates a delay signal for every period obtained by carrying out L (L being two or more integers) division of the transformer drive period Tj, and outputs each clock signal to each switching circuit section to the timing of this delay signal. this time -- each -- the phase of the clock with which switching circuit (section m) (m is supplied to 1 <=m<=n and integer) of arbitration is expressed with any of {phi+ (0 degree - 360 degrees)} they are. The period of the ripple current is expressed as Tj (j is the integer of 1 <=j<=k and arbitration).
[0039] In the conventional high-voltage transformer assembly, the sum total ripple current [drawing 6 (B)] in n= 2 was twice [about] the ripple current [drawing 6 (A)] in n= 1. However, according to the gestalt of this operation, the phase of the ripple current value which flows to each electrolytic capacitor Cm can be set as arbitration. Therefore, each period Tj and a phase can be set up free so that it may become below a ripple current value in case the sum total of a ripple current value which flows to an electrolytic capacitor Cm is n= 1. Moreover, it can make it possible to own two or more ripple currents with the same phase, and can also avoid that the period of the ripple current becomes too much early.
[0040] That is, it made it possible to equalize the ripple current with the whole electrolytic capacitor by preparing time difference (phase) in each ripple current which was flowing in phase and this period to each electrolytic capacitor Cm conventionally.
[0041]
[Effect of the Invention] [as explained in full detail above, when a transformer drive circuit is constituted from the n switching circuit sections (1-n) according to this invention] The sum total of a ripple current value which flows to the electrolytic capacitor Cm (1 <=m<=n) in the switching circuit section (m) It can be made smaller than the ripple current which flows to the electrolytic capacitor C1 in n= 1, and, moreover, the sum total of this ripple current value can be decreased more by enlarging n.
[0042] That is, by preparing time difference (phase) in each ripple current which was flowing in phase

and this period to each electrolytic capacitor conventionally, the ripple current which flows to the whole electrolytic capacitor could decrease the electrolytic capacitor capacity which is equalized, therefore is needed, and made the cost cut possible.

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* NOTICES *

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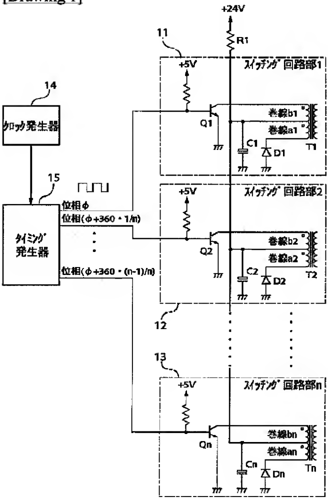
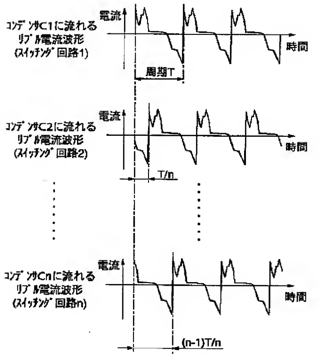
3.In the drawings, any words are not translated.

DRAWINGS

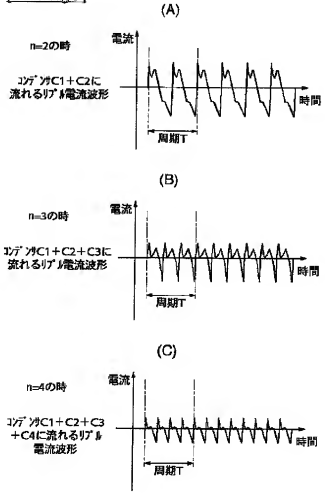
[Drawing 1]



[Drawing 2]



[Drawing 3]



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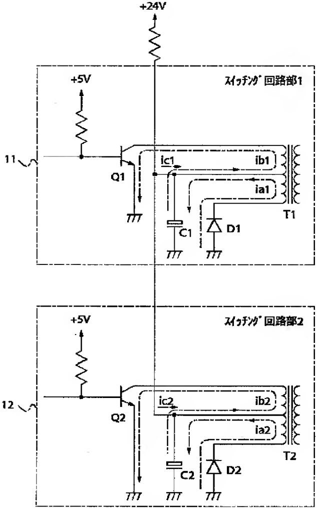
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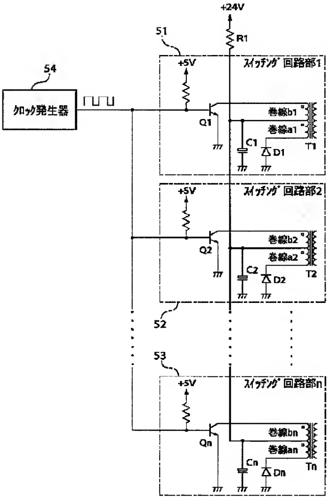
Q1
ic1
ib1
ia1
T1
C1
D1
+5V
ｽｲｯﾁﾝｸﾞ回路部2
12
Q2
ic2
ib2
ia2
T2
C2
D2

[Drawing 5]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54
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巻線b1
巻線a1
C1
D1
T1
+5V
スイッチング回路部2
Q2
巻線b2
巻線a2
C2
D2
T2
52
53
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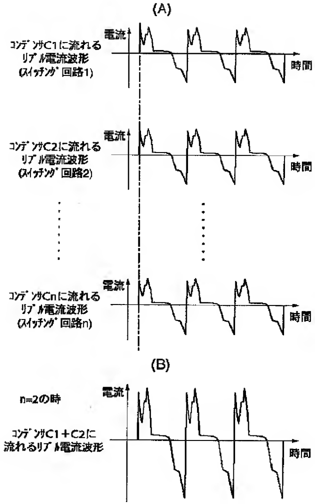
スイッチング回路部n
Qn
巻線bn
巻線an
Cn
Dn
Tn

[Drawing 6]


(A)
電流
ｺﾝﾃﾞﾝｻC1に流れる
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(ｽｲｯﾁﾝｸﾞ回路1)
時間
電流
ｺﾝﾃﾞﾝｻC2に流れる
ﾘﾌﾟﾙ電流波形
(ｽｲｯﾁﾝｸﾞ回路2)
時間
電流
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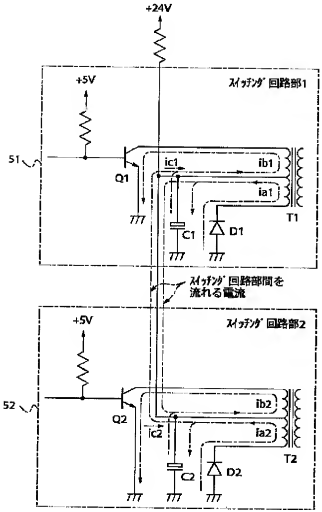
ﾘﾌﾟﾙ電流波形
(ｽｲｯﾁﾝｸﾞ回路n)
時間
(B)
n=2の時
電流
ｺﾝﾃﾞﾝｻC1＋C2に
流れるﾘﾌﾟﾙ電流波形
時間

[Drawing 7]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51
Q1
ic1
ib1
ia1
T1
C1
D1
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流れる電流
+5V
ｽｲｯﾁﾝｸﾞ 回路部2
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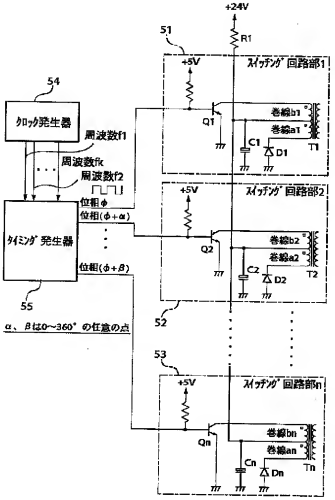
ib2
ic2
ia2
T2
C2
D2

[Drawing 8]



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